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Compatibility Assessment of CVD Growth of Carbon Nanofibers on Bulk CMOS Devices

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ABSTRACT

We compare the level of deterioration in the basic functionality of individual transistors on ASIC chips fabricated in standard 130 nm bulk CMOS technology when subjected to three disparate CVD techniques with relatively low processing temperature to grow carbon nanostructures. We report that the growth technique with the lowest temperature has the least impact on the transistor behavior.

Carbon nanotubes (CNTs) and nanofibers (CNFs) are attractive materials for many electronic nanodevices due to their extraordinary electrical and mechanical properties.[1–3] Many processes have been proposed to grow this material. Among those, chemical vapor deposition (CVD) is favorable in many applications due to the possibility of growth direction alignment[4–7] as well as precise control over growth position by patterning the catalyst material.[8,9] However, to harness the full potential of carbon nanostructures, we need to achieve not only a scheme to fabricate excellent carbon materials but also a method to allow these to become an integral part of mainstream circuitry. The technological challenges faced when developing the process sequence for the fabrication of new generations of integrated circuits are very large, and the motivation for a major change, such as introducing carbon nanostructures, requires not only promises of significant added value and functionality but also a very robust promise of technological process compatibility. For instance, the authors are pursuing realization of a variable capacitor (Varactor) based on vertically aligned CNFs for radio frequency applications (see Figure 1). As the system frequency increases, the spatial arrangement of the components with respect to each other becomes essential and therefore closely integrating the carbon-based devices to the rest of circuitry, e.g., on top of the CMOS chip, is inevitable in this frequency range. One step toward realizing such a system is to demonstrate the lack of deterioration of existing electronic devices in the integrated circuit on which the growth of carbon nanostructures is carried out.

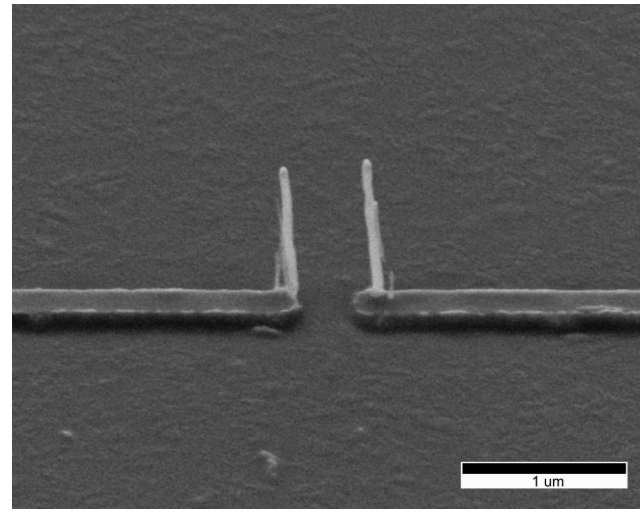

Figure 1. VACNF-based variable capacitor (Varactor) for RF application as an example of the significance of closely integrating the carbon-based nanostructure to the readout circuitry.

It has been shown by Haque et al.[10] that PECVD and CVD growth of carbon nanotubes are compatible with CMOS devices on high temperature SOI substrates having tungsten as an interconnect metal. However, the presence of aluminum metallization in bulk CMOS technology jeopardizes this compatibility due to the low melting point of aluminum, unless the growth temperature is decreased. There have been

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Table 1. Summary of Growth Parameters[a]

process steps	parameters	DC-PECVD	RF-PECVD	thermal CVD
catalyst pretreatment	temperature		560 °C	610 °C
	duration		15 min	20 min
	gas phase		H_2	H_2
growth	temperature	500 °C	560 °C	610 °C
	duration	60 min	60 min	2 min
	gas phase and carbon source	C_2H_2/NH_3	graphite (solid carbon supply)/H_2	C_2H_2/He
	plasma source	DC	RF	N.A.

[a] No catalyst pretreatment was performed in the case of DC-PECVD growth.

several reports on carbon nanotubes and -fibers grown at substrate temperatures as low as 120 °C.[11–13] However, the actual growth temperatures at the surface could be considerably higher due to the plasma heating.[14] Moreover, there is still not enough information on the electronic and mechanical properties of such nanofibers to make a promising prognosis of the performance of the device incorporating them. Alternatively, carbon nanotubes or -fibers can be grown on a proper substrate at high temperatures separately and then be released and transformed to a receptor substrate in a low temperature process.[15,16] However, in a device such as our VACNF-based Varactor, the unknown mechanical stability at the contact point to the new substrate could impose considerable degradation in the final device performance as well as in the fabrication yield.

We have employed three disparate CVD growth environments, known to yield vertical CNFs or CNTs on Si-based substrates, with aggressively scaled down growth temperatures (500−610 °C) which enabled us to assess the possible transistor deterioration induced during radically different growth conditions. First we show that the growth materials and their deposition and patterning techniques are compatible with the underlying bulk CMOS circuitry and then we assess the deterioration in the basic functionality of the circuitry after growing carbon nanostructures. We have used Ni/W as the catalyst/underlayer stack in our study due to its simplicity in fabrication, being widely used, and its material compatibility to standard CMOS processes.[17]

ASIC (Application Specific Integrated Circuit) chips employed for this experiment were fabricated in 130 nm node standard bulk CMOS technology and contained electronic components and circuitry as well as individual transistors. The individual transistors which were the subject of our study were four-fingered PMOS and NMOS transistors (W/L = 4 × 5.0 μm/0.37 μm) having 2 nm thick gate oxide with separate aluminum contact pads providing direct access to each transistor terminal. A top passivation layer consisting of 500 nm silicon dioxide plus 600 nm silicon nitride

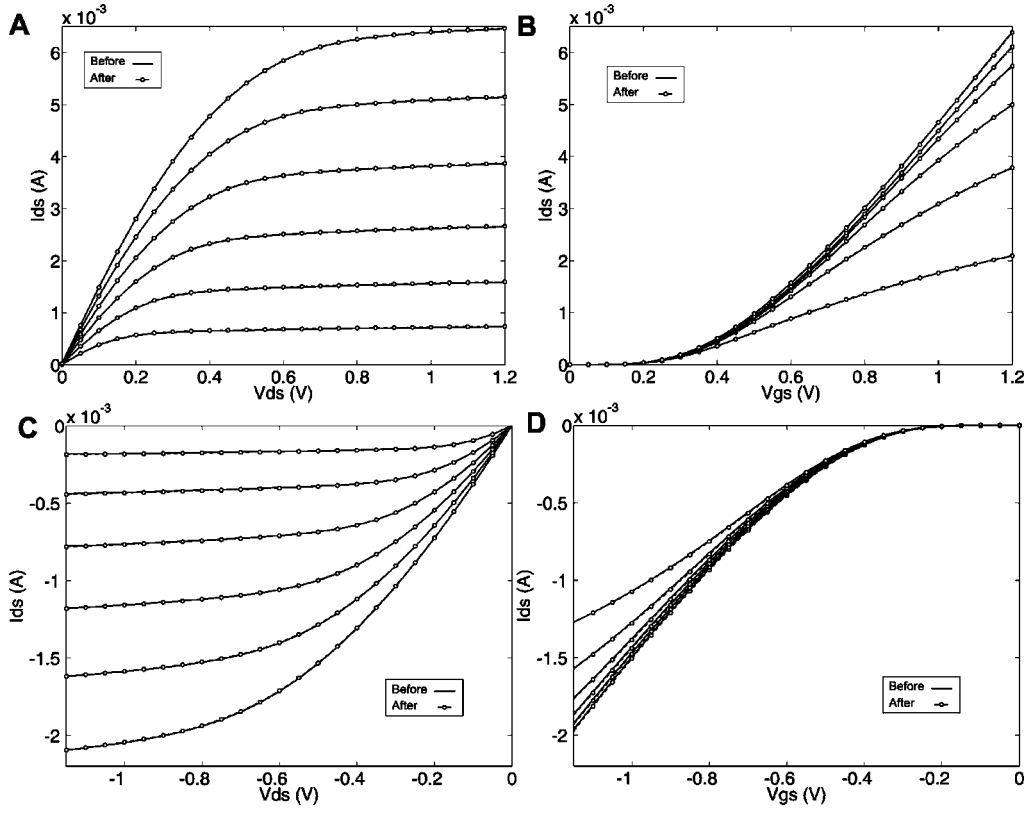

Figure 2. $I-V$ characteristics of individual transistors, before and after pregrowth processing, are compared. (A) $I_{ds}-V_{ds}$ in NMOS transistors for 6 different gate voltages.(B) $I_{ds}-V_{gs}$ in NMOS transistors for 6 different drain voltages. (C) $I_{ds}-V_{ds}$ in PMOS transistors for 6 different gate voltages. (D) $I_{ds}-V_{gs}$ in PMOS transistors for 6 different drain voltages.

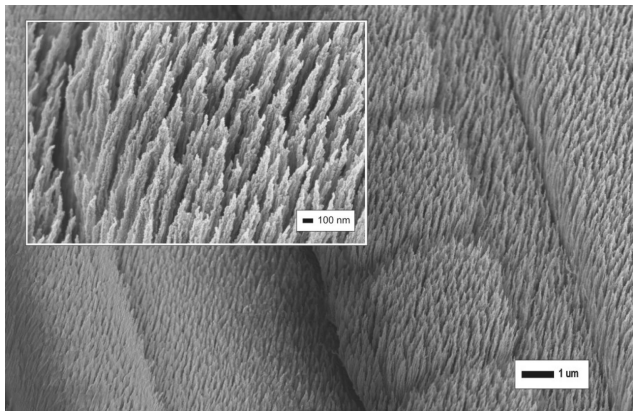

Figure 3. SEM micrograph of the DC-PECVD growth result on top of an ASIC chip. The inset shows formation of carbon nanofiber bundles covered by amorphous carbon.

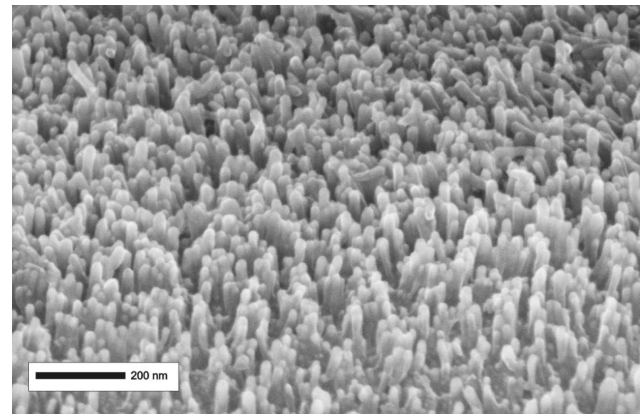

Figure 4. Very short and densely populated carbon nanofibers grown on top of an ASIC chip after the RF-PECVD growth process.

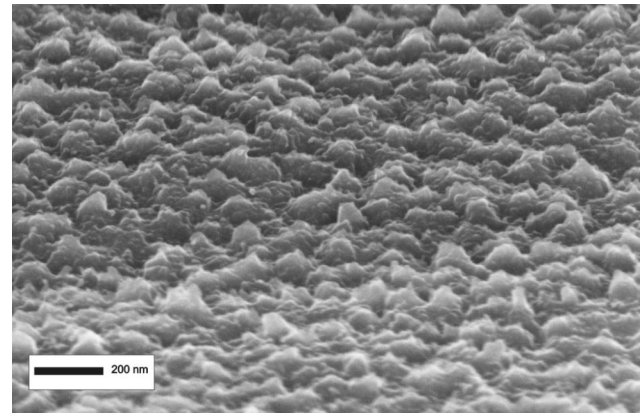

Figure 5. Thermal CVD process on top of an ASIC chip resulting in a localized catalytic (Ni) film instead of tubular carbon structures.

protected the electronics on the ASIC chips. To sustain the electrical contacts to the individual transistors, we patterned the catalyst/underlayer metals to prevent any deposition on top of the contact pads. Standard photolithography was used for this purpose although it was very challenging due to the small size of the individual ASIC chips (1 mm by 1 mm). The small size makes it challenging to spin the photoresist uniformly on top of the chip due to the amplified edge effect. To solve the problem, the photoresist (Shipley S-1813) was diluted in Ethyl Lactate to reduce the surface tensions in the solution. The solution was spun two times for a relatively long time (3 min) to let the excess solvent dry out. The spun photoresist was soft-baked at 55 °C after the first spinning step and at 110 °C after the second one, both for 90 s on a hotplate. A 50 nm thick tungsten (W) layer was then deposited on top of the patterned photoresist in a DC-magnetron sputtering system using argon as sputtering gas at 5 mTorr and a plasma power of 300 W. The processing was continued by deposition of a 10 nm thick nickel (Ni) film in an e-beam evaporation system at 3.0×10^{-6} mbar. Finally, the pattern was transferred to the metallic stack in a lift-off process.

Subsequently, every chip with patterned metallic stack on top was employed for one CVD growth technique; direct current plasma-enhanced (DC-PECVD), radio frequency plasma-enhanced (RF-PECVD), and thermal CVD.

In the DC-PECVD method the chips were attached to a grounded cathode that contained an ohmic heater. Then the chips were heated up to the growth temperature in a low vacuum of 10^{-3} Torr. After substrate heating, a voltage was applied to the anode at the same time as the gas mixture was introduced. The gas flow and the chamber pressure were kept constant through automatic regulation during the growth. The RF-PECVD and the thermal growth processes were performed in a same vertical hot wall Plassys reactor, previously described,[18,19] consisting of a quartz bell-jar chamber heated by two independent resistive coils. The chips were placed on a graphite 250 mm diameter sample-holder, which was RF-polarized and innovatively used as a single carbon supply in the case of the PECVD technique. The two growth processes consisted of two consecutive steps performed at the same processing temperature. First, an annealing pretreatment was performed under a reductive H2 atm to form Ni catalyst nanoparticles from the initial thin Ni film ("dewetting step"); then, the growth occurred from these germs by introducing acetylene (C2H2) diluted in helium (He) for the thermal CVD growth mode, or by igniting a RF glow discharge above the graphite sample-holder in a pure H2 atm, for the RF-PECVD growth technique. The summary of growth conditions in each process are listed in Table 1.

The electrical characterization of each individual MOS transistor comprises measurements of drain current versus drain voltage ($I_{ds}-V_{ds}$) and versus gate voltage ($I_{ds}-V_{gs}$). These characteristic curves give an overview of the deterioration in the static performance of the individual transistors caused by a specific growth process. To assess the level of deterioration and to compare the influence of each growth process, two parameters were used: the on-state drain current and the gate leakage current. We measured the on-state source-drain current in each NMOS transistor while applying 1 V to the drain and the gate contacts and grounding the source and the bulk terminals. In the case of PMOS transistors −1 V was applied to the drain and the gate. The gate leakage current was measured while grounding the

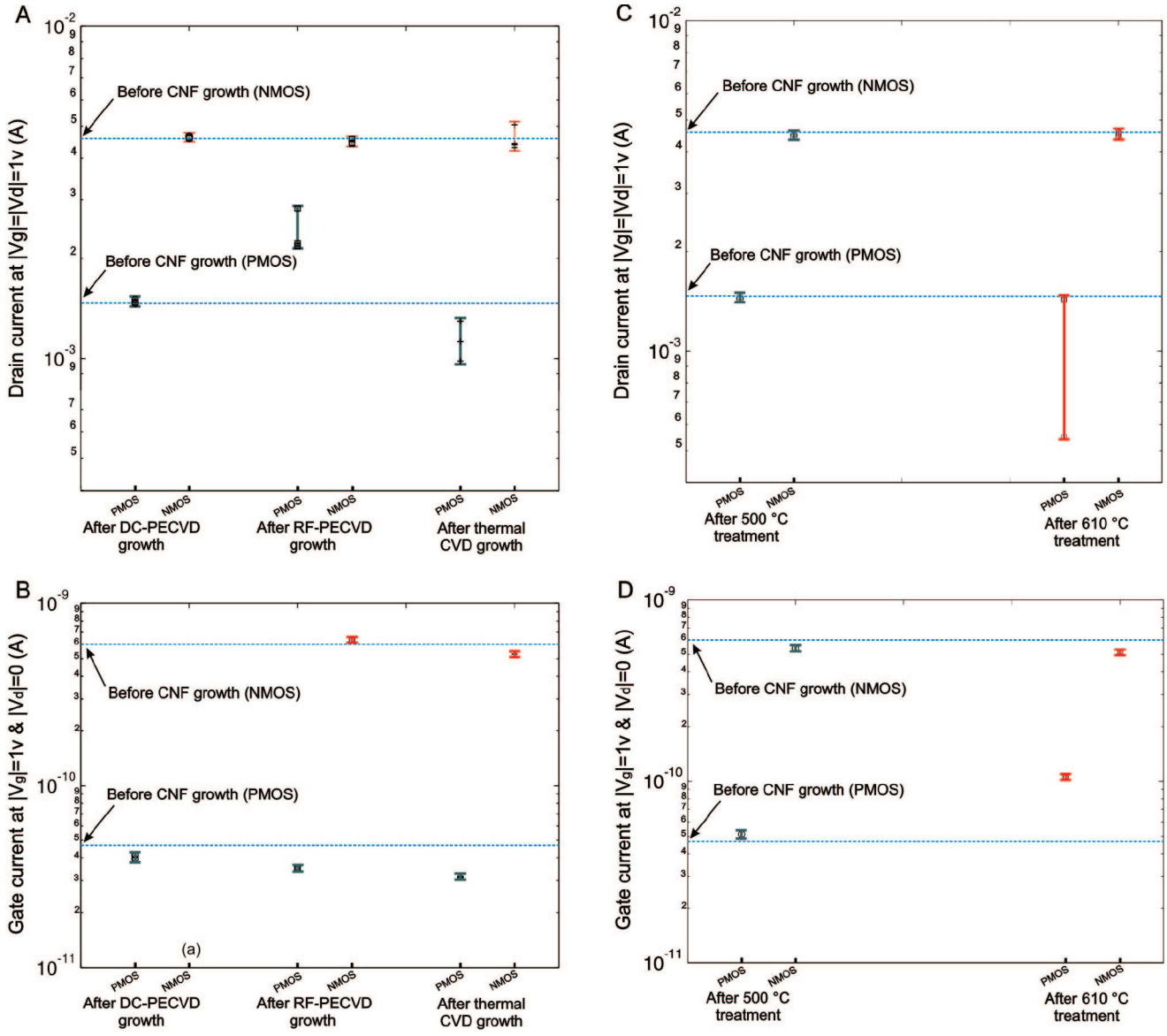

Figure 6. Deterioration of (A) on-state drain current and (B) gate current of PMOS and NMOS transistors after three disparate growth processes. The effect of thermal treatment on (C) on-state drain current and (D) gate current of transistors. The actual NMOS transistor gate current is small enough when compared to parasitic surface current due to amorphous carbon deposits in the PECVD growth process to be obscured and inaccessible for direct observation.

source, drain, and bulk contacts and applying +1 and −1 V to the gate terminal in NMOS and PMOS transistors, respectively. The electrical measurements employed a Keithley 4200 Semiconductor Characterization System with a self-voltage source equipped with 4200-PA remote preamplifier for low current measurements. The transistors were measured at room temperature in a nitrogen purged Cascade Summit 12661B probe station mounted on a vibration-isolated table.

Three ASIC chips, each containing four PMOS and four NMOS individual transistors, were fully examined in their pristine state. They were subsequently examined after finalizing the pregrowth processing and these measurements were also repeated after the growth. The results of each growth method were also imaged using a Leo Ultra 55 FEG scanning electron microscope (SEM).

As seen from Figure 2A−D, no considerable change is observed in the drain current characteristics of either NMOS or PMOS transistors after performing the pregrowth processing. This can be translated to CMOS compatibility in terms of the growth materials and the required deposition/patterning processes.

The result of DC-PECVD growth is shown in Figure 3: a uniform growth all over the chip surface even on the spots where no catalyst was deposited is observed. The inset of Figure 3 shows that the grown nanofibers have formed small bundles, which then were covered by amorphous carbon deposits. These are most likely the results of deviation from the standard growth temperature (700 °C) to a lower temperature (500 °C). The RF-PECVD growth has resulted in patterned highly dense forests of thin and short nanofibers as shown in Figure 4. Despite the fact that the catalyst (Ni)

film is 10 nm thick, the CNF mean diameter is very small (about 20 nm). We believe that the "dewetting step" of Ni above W is responsible for these low dimensions. As explained in ref 18, this growth process does not favor thin catalytic film due to parasitic CNF etching phenomena resulting from sample bombardment by H^+ ions. This also explains the limited CNFs mean height observed in Figure 4 (about 130 nm). No parasitic growth and no amorphous carbon deposition have been observed in this case. The thermal CVD process (see Figure 5) has not produced CNTs or CNFs but a localized catalytic film above W with no sign of parasitic growth on unpatterned areas. The nature of this film has not been identified yet but it should be based on C and perhaps W. A particular interaction of materials under investigation (Ni, W, and C) at the processing temperature (610 °C) has prevented the growth of carbon tubular structure.

Figure 6 compares the on-state drain current and the gate leakage current of all 8 transistors on each ASIC chip after the growth of carbon nanofibers to the corresponding values obtained in the pristine state. As shown in Figure 6A, the DC-PECVD technique which has the lowest growth temperature has the least influence on the on-state drain current in both NMOS and PMOS transistors. The deterioration is more severe for RF-PECVD and thermal CVD techniques especially in PMOS transistors. The gate current measurements as depicted in Figure 6B corroborate the minimal impact of DC-PECVD growth for PMOS transistors. In the case of NMOS transistors, however, we measured gate currents in the range of milliamperes. This would be an unreasonably large current if it passed through the gate insulator of these functional transistors (as demonstrated in Figure 6A); we attribute it to conduction through the parasitic surface paths to the gate pad created due to the parasitic growth and amorphous carbon deposits. The actual NMOS transistor gate insulator current on the DC-PECVD chip is thus small enough to be obscured and inaccessible for direct observation; the circumstantial evidence of little impact on any of the gate currents together with robust output characteristics for these particular transistors leads us to conclude that the gate insulator current most likely is very close to its pristine value. Finally, it should be mentioned that one PMOS transistor stopped being functional after the thermal CVD growth (highest growth temperature).

In addition, a sole thermal treatment was performed on two pristine chips in a vacuum with the same thermal budget as the DC-PECVD (500 °C, 60 min) and the thermal CVD (610 °C, 22 min) growth modes that were the lowest and the highest thermal budgets, respectively. As expected from the previous results, no considerable change was observed in the gate and drain currents of the transistors on the chip subjected to the lowest thermal budget (see Figures 6C,D). On the other hand, the gate current of the PMOS transistors on the chip subjected to the highest thermal budget was almost doubled. A substantial degradation is also visible in the on-state drain current of one of the same PMOS transistors as shown in Figure 6C. The similarity of the results obtained from sole thermal treatment to those of growth modes substantiates the significance of the thermal budget among other parameters in degradation of the transistors performance.

In summary, we have assessed and compared the deterioration in basic functionality of bulk CMOS transistors on ASIC chips fabricated in standard 130 nm technology when subjected to three disparate CVD growth techniques with different growth temperatures. We have found that the level of transistor deterioration is very small for DC-PECVD which requires the lowest processing temperature (500 °C). This particular growth technique thus shows promise to deliver CMOS compatible carbon nanostructures. For future realization of CMOS integrated carbon nanofiber devices it remains to be validated that we can develop these techniques to grow high-quality carbon nanofibers that display the properties required for functional nanoelectromechanical devices.

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